Soft Switching of Multioutput Flyback Converter with Active Clamp Circuit

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ABSTRACT: This paper presents achieving soft switching in multioutput flyback converter with active clamp circuit for power supplies. The flyback converter operated at 100 KHz in CCM mode. This provides output voltages (positive and negative), lower and higher voltages than input voltage. With the help of active clamp circuit, the transformer leakage energy is recycled, and zero-voltage-switching (ZVS) for primary main switch is achieved.

Keywords— multioutput flyback converter, active clamp, continuous conduction mode , ZVS

I. INTRODUCTION
Fly-back converter is the most commonly used SMPS circuit for low output power applications. Compare to other topologies in [1],[2], fly-back is simple, less components and low cost. A fly-back converter topology is widely used in application below 100W. They are especially popular in multi-output applications, due to the low parts count only one diode and capacitor per output is required. In a fly-back converter, when more than one output is present, the output voltages track one another with the input voltage and the load changes, far better than they do in the forward converter. This is because of the absence of the output inductor, so the output capacitor connects directly to the secondary of the transformer and acts as a voltage source during the turned off period of the switch. So it is essential to design a fly-back converter to get a multiple output with improved performance and compact size using [3],[4]. In this paper multi output active clamp fly-back converter topology for power supplies is designed. The switch in the fly-back converter is operated at hard switching. Therefore the voltage and current stress of switch suffered from the transformer leakage inductance is very high and also an EMI problem from the hard switching limit the power rating for higher power application [5],[6]. To overcome these drawbacks and to achieve ZVS, an active clamp circuit is added in multioutput fly-back converter. Active clamping is an effective means to clamp the voltages across semiconductor devices as well as to achieve soft switching [7]-[9]. The active-clamp circuit provides the benefits of recycling the transformer leakage energy while minimizing turn-off voltage stress across the power switch [10]-[11]. In addition, the active-clamp circuit provides a means of achieving zero-voltage-switching (ZVS) for the power switch and subsequent lowering of the output rectifier di/dt. This results in decreased rectifier switching loss and output switching noise.

The analysis, design and implementation of a 70W active clamp fly-back converter is presented in this paper to achieve zero voltage switching (ZVS) for main switch. With the auxiliary switch, clamp capacitor and resonant inductor, the surge energy stored at the leakage inductance can be recycled by the active clamp circuit.

II. ACTIVE CLAMP FLYBACK CONVERTER ANALYSIS
Fig: 1 shows the block diagram of multioutput active clamp fly back converter. Fig. 2 shows the circuit configuration of the active clamp flyback converter. The magnetizing inductance is represented as $L_m$. The resonant inductance $L_r$ is the sum of transformer leakage inductance and external inductance. The resonant capacitance $C_r$ is equal to the parallel combination of the parasitic capacitance of main switch $S_{main}$ and auxiliary switch $S_{aux}$. The auxiliary switch $S_{aux}$ and clamp capacitor $C_{clamp}$ represent the active clamp circuit to recycle absorb the surge energy due to the leakage inductance so as to reduce the voltage stress of main switch $S_{main}$. The resonant capacitance $C_r$ and inductance $L_r$ are resonant to achieve ZVS operation for main switch $S_{main}$. Before the system analysis, some assumptions are made as: (1) The resonant period
generated by the clamp capacitance $C_{\text{clamp}}$ and resonant inductance $L_r$ is greater than turn off time of main switch; (2) The resonant inductance is less than magnetizing inductance ($L_r < L_m$); (3) All semiconductors (switches and diodes) are ideal; (4) the converter is operated in the continuous conduction mode; (5) the energy stored in the resonant inductance is greater than energy stored in the resonant capacitance in order to achieve ZVS operation for main switch.

Fig. 1. Block diagram of active clamp multioutput flyback converter

Fig. 2. Active clamp flyback converter

Fig. 3. Active-clamp flyback topological states
Fig 3 and Fig 4 shows necessary equivalent circuits for each interval and waveforms respectively. In fig 4 during interval \((T0-T1)\): At \(T0\), switch \(S_{main}\) is on, and the auxiliary switch \(S_{aux}\) is off. The output rectifier, \(D_1\), is reversed biased. The magnetizing inductance is being linearly charged as it charges in "normal" flyback operation.

In the interval \((T1-T2)\): \(S_{main}\) is turned off at \(T1\). \(C_r\) is charged by the magnetizing current which is also equal to the current through the resonant inductor. Consequently, the voltage appearing across the magnetizing inductance, \(V_{pri}\), decreases as \(V_{clamp}\) increases, according to the voltage divider action, \(V_{pri} = -V_{clamp}(L_m/L_r+L_m)\).

During the interval \((T2-T3)\): At \(T2\), switch \(S_{main}\) is on, and the auxiliary switch \(S_{aux}\) is off. The output rectifier, \(D_1\), is reversed biased. The magnetizing inductance is being linearly charged as it charges in "normal" flyback operation.

In the interval \((T3-T4)\): At \(T3\), primary voltage \(V_{pri}\) has decreased to the point where the secondary transformer voltage is sufficient to forward bias \(D_1\). The transformer primary voltage is then clamped by the output capacitance to approximately \(NV_o\). \(L_r\) and \(C_{clamp}\) begin to resonate. In order for \(S_{aux}\) to achieve ZVS, the device should be turned on before clamp capacitor current \(I_{clamp}\) reverses direction.

During the interval \((T4-T5)\): The auxiliary switch, \(S_{aux}\), is turned off at \(T4\), effectively removing \(C_{clamp}\) from the circuit. A new resonant network is formed between the resonant inductor and the MOSFET parasitic capacitances of main switch. The transformer primary voltage remains clamped at \(NV_o\) as \(C_r\) is discharged.

In the interval \((T5-T6)\): Assuming the energy stored in \(L_r\) is greater than the energy stored in \(C_r\), At \(T5\) \(C_r\) will be sufficiently discharged to allow \(S_{aux}\)’s body diode to start conducting. The voltage across the resonant inductor becomes clamped at \(V_{in} + NV_o\).

During the interval \((T6-T7)\): \(S_{main}\) is on, and the secondary current is decreasing as the resonant inductor current increases. At \(T7\), the secondary current decreases to zero (because the resonant inductor current has equalled the magnetizing current), and \(D_1\) reverse biases, allowing the polarity to reverse on the transformer primary. The magnetizing and resonant inductances begin to linearly charge again, starting another switching cycle.
III. DESIGN PROCEDURE

- The turn ratio between the transformer primary side and secondary side is equal to
  
  \[ N = \frac{N_1}{N_2} = \frac{V_{in,max}}{V_o (1 - D_{max})} \]  
  \[ \text{ ................................................................. (1)} \]

  If the clamp capacitance is large enough, the voltage across resonant inductor is neglected.

- Magnetizing inductance,
  
  \[ L_m = \frac{n[V_{in,max}]^2}{2P_o (min) \tau_{sw}} \]  
  \[ \text{ ................................................................. (2)} \]

- Peak current of the main switch
  
  \[ I_{main,peak} = \frac{P_o}{\eta V_{in,min} \cdot D_{max}} + \frac{V_{in,min}}{L_m} \cdot D_{max} \tau_{sw} \]  
  \[ \text{ ................................................................. (3)} \]

- Voltage stress of rectifier diode
  
  \[ V_{D0,max} = V_{in,max} \frac{N}{N} + V_o \]  
  \[ \text{ ................................................................. (4)} \]

- Peak secondary diode current.
  
  \[ I_{D0,peak} = \frac{2P_o}{V_o (1 - D_{max})} \]  
  \[ \text{ ................................................................. (5)} \]

- Output capacitance is given by,
  
  \[ C_o = \frac{D_{max} P_o}{f_{sw} V_o \delta V_o} \]  
  \[ \text{ ................................................................. (6)} \]

  Where \( V_{out,ripple} = 1\% \) of \( V_o \).

- Resonant capacitance : \( C_r = \) parallel combination of the parasitic capacitance of main switch \( S_{main} \) and auxiliary switch \( S_{aux} \).

- Resonant inductor \( L_r \) is given by,
  
  \[ L_r = \frac{1}{4\pi^2 f_r \cdot C_r} \]  
  \[ \text{ ................................................................. (7)} \]

- Clamp capacitance is given by,
  
  \[ \frac{[(1 - D_{min} \tau_{in}) \tau_{sw}]}{\pi^2 L_r} \]  
  \[ \text{ ................................................................. (8)} \]
where $D_{\text{min}} = \frac{D_{\text{max}} \cdot V_{\text{in}}}{V_{\text{max,min}}}$

A. Experimental result

A 70W proposed circuit is designed and simulated using Orcad Pspice 9. Fig.5 shows the simulation circuit of multioutput active clamp flyback converter. Table 1 and Table 2 gives the simulation and hardware results. Fig.(6)and (7) shows the experimental waveforms of the gate-to-source voltages of main switch and auxiliary switch of main switch. The time delay between the auxiliary switch turn-off and main switch turn-on to ensure main switch turn on at ZVS respectively. Fig.(8) gives the experimental waveforms of gate signals of main switch $V_{\text{smain,gs}}$ and auxiliary switch $V_{\text{saux,gs}}$ and transformer primary voltage $V_{\text{pri}}$. When main switch is turned on, the transformer primary side voltage is equal to Vin. If the main switch is turned off, the primary side voltage equals $-N \cdot V_{\text{o}}$. Fig. (9) shows the gate-to-source and drain-to-source voltage for main switch. Before the mains switch is turned on the drain-to-source voltage has been reached zero. Fig.(10) gives the switch $V_{\text{smain,gs}}$ and auxiliary switch $V_{\text{saux,gs}}$ and transformer experimental waveform of clamp capacitor voltage.

![Simulation Circuit](image)

**Fig. 5. Simulation circuit**

<table>
<thead>
<tr>
<th>TABLE 1</th>
<th>SIMULATION RESULT</th>
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<tr>
<td>$V_{\text{o1}}$</td>
<td>$V_{\text{o2}}$</td>
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<td>Required outputs (V)</td>
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<td>Obtained output voltage (V) for full load</td>
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<td>Obtained output voltage (V) for no load</td>
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<th>TABLE 2</th>
<th>HARDWARE RESULT</th>
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<tbody>
<tr>
<td>$V_{\text{o1}}$</td>
<td>$V_{\text{o2}}$</td>
</tr>
<tr>
<td>Required outputs (V)</td>
<td>6.3</td>
</tr>
<tr>
<td>Obtained output voltage (V) for full load</td>
<td>6.4</td>
</tr>
<tr>
<td>Obtained output voltage (V) for no load</td>
<td>6.5</td>
</tr>
</tbody>
</table>
Fig. 6. The gate-to-source voltages of main switch(yellow) in channel 1 and gate to source voltage of auxiliary switch(pink) in channel 3.

Fig. 7. The time delay between the auxiliary switch(pink in channel 3) turn-off and main switch(yellow in channel 1) turn-on to ensure main switch turn on at ZVS.

Fig. 8. The gate-to-source voltages of main switch(yellow) in channel 1 and gate to source voltage of auxiliary switch(pink) in channel 3. And the transformer primary voltage Vpri(blue) in channel 2 and primary current Ipri (green) in channel 4
IV. CONCLUSIONS

The operation of 70W active clamp flyback converter for multioutput analysed. The proposed circuit is designed and tested and the required multioutput output voltages are obtained. The energy stored in transformer leakage inductance is recycled. This benefits allow power converter designers to achieve ZVS and reduces voltage stress on switch.
REFERENCES

[10] Analysis, design and implementation of an active clamp flyback converter 2005 IEEE